VLSI-SoC 2019 Program

Sunday 6, october	
15:00 - 16:00 h.	Steering Committee Meeting
16:00 - 18:00 h.	Technical Program Committee Meeting
18:00 - 19:30 h.	IFIP Working Group 10.5 Meeting

Monday 7, october		
8:00 - 17:00 h	Registration of participants	
08:40 - 09:00 h.	Opening ceremony	
09:00 - 10:00 h.	**Keynote 1: *Open, Secure, Near-Sensor Analytics: A Parallel Ultra-Low Power (PULP) Approach*** **Luca Benini** **Chair: Giovanni De Micheli**	
10:00 - 10:30 h.	Coffee break	
	Session 1: Innovations in IC Design in FDSOI CMOS (Chair: Andrei Vladimirescu)	Session 2: Circuits and Systems for SignalProcessing and Communications (Chair: H. Fatih Ugurdag)
10:30 - 10:50 h.	New design of analog and mixed-signal cells using back-gate cross-coupled structure	An Associativity-Agnostic in-Cache Computing Architecture Optimized for Multiplication

10:50 - 11:00 h.	A Distributed Body-Biasing Strategy for Asynchronous Circuits	Hardware Considerations for Selection Networks
11:00 - 11:30 h.	Benefits of an FD-SOI Feature: Optimal Power Budget of Wireless Links through Phase Noise Tuning	A Mixed-Signal Offset-Compensation System for Multi-Gbit/s Optical Receiver Frontends
11:30 - 11:50 h.	Does FDSOI bring added value for new connectivity challenges?	Lossless Look-Up Table Compression for Hardware Implementation of Transcendental Functions
12:00 - 14:00 h.	Lunch	
14:00 - 15:00 h.	**Invited talk 1: *Designing Application Specific Machine Learning/Deep Learning Cores*** **Claudionor Coelho** **Chair: Carlos Silva-Cardenas**	
	Session 3: Computer-Aided Design (Chair: Srinivas Katkoori)	Session 4: Variability, Reliability and Test 1 (Chair: Matteo Sonza Reorda)
15:00 - 15:20 h.	Automated Synthesis of Multi-Port Memories and Control	Software-Based Self-Test for Transition Faults: a Case Study
15:20 - 15:40 h.	Approximate Arithmetic Circuit Design Using a Fast and Scalable Method	Implementation-Independent Functional Test Generation for RISC Microprocessors
15:40 - 16:00 h.	An ILP-based Optimization Method for Radiation Hardened Register and ECC Mixed 146 Architectures	Minimum Energy FinFET Schmitt Trigger Design Considering Process Variability
16:00 - 16:50 h.	Poster Session + Coffee break	
16:50 - 18:10 h.	Young Professional + SIGDA Diversity Session	
19:30 h.	Welcome cocktail	

Tuesday 8, october		
09:00 - 10:00 h.	**Keynote 2: *Solving Scalability Problems in EDA by Using Optimization and Machine Leaning*** **Lelah Behjat** **Chair: Pierre Emmanuel Gaillardon**	
10:00 - 10:30 h.	Coffee break	
	Session 5: Special Session: Silicon-Proven Multiprocessor SoC Design Strategies (Chair: Gerhard Fettweis)	Session 6: Prototyping (Chair: Graziano Pravadelli)
10:30 - 10:50 h.	Challenges and Solutions for Future-Proof Embedded Vision and AI Processors	Engineering of an Effective Automatic Dynamic Assertion Mining Platform
10:50 - 11:00 h.	A 0.80 pJ/flop, 1.24 Tflop/sW 8-to-64 bit Transprecision Floating-Point Unit for a 64 bit RISC-V Processor in 22 nm FD-SOI	SEARS: A Statistical Error and Redundancy Analysis Simulator
11:00 - 11:30 h.	KAVUAKA: A Low Power Application Specific Hearing Aid Processor	Non-intrusive Fault Injection Techniques for Efficient Soft Error Vulnerability Analysis
11:30 - 11:50 h.	5G-and-Beyond Scalable Machines	Domain-Specific Architecture for IMU Array Data Fusion
12:00 - 14:00 h.	Lunch	
14:00 - 15:00 h.	**Invited talk 2: *5G Radio Frequency Front-End: be wide-band, be low-power, be low-cost !*** **Francois Rivet** **Chair: Ricardo Reis**	
	Session 7: Embedded Systems Design	Session 8: Low-power and Analog IC Design (Chair: Alberto

	(Chair: Michael Huebner)	Macii)
15:00 - 15:20 h.	SURF: Self-aware Unified Runtime Framework for Parallel Programs on Heterogeneous Mobile Architectures	The Impact of Turbo Frequency on the Energy, Performance, and Aging of Parallel Applications
15:20 - 15:40 h.	Arbitrary-Precision Convolutional Neural Networks on Low-Power IoT Processors	Performance Analysis of a Comparator Based Mixed-Signal Control Loop in 28 nm CMOS
15:40 - 16:00 h.	PhD Forum Introduction	
16:00 - 16:50 h.	PhD Forum+ Student Forum + Coffee break	
16:50 - 18:20 h.	Industry Panel: "Digital transformation: key enabling technologies and their industrial perspectives"	
19:30 - 22:00 h.	Gala Dinner	

Wednesday 9, october		
09:30 - 10:30 h.	**Keynote 3: *Electronic Design Automation and Machine Learning Hardware*** **Raul Camposano** **Session Chair: Victor Grimblatt**	
10:30 - 11:00 h.	Coffee break	
	Session 9: Emerging Technologies (Chair: Ian O'Connor)	Session 10: Variability, Reliability and Test 2 (Chair: Salvador Mir)
11:00 - 11:20 h.	A Product Engine for Energy-Efficient Execution of Binary Neural Networks Using Resistive Memories	Evaluation of SET under Process Variability on FinFET Multi-level Design

11:20 - 11:40 h.	Memory Sizing of a Scalable SRAM In-Memory Computing Tile Based Architecture	A Simplified Layout-Level method for Single Event Transient Faults Susceptibility on Logic Gates
11:40 - 12:00 h.	A Predictive Process Design Kit for Three-Independent-Gate Field-Effect Transistors	An NBTI-Aware Digital Low-Dropout Regulator with Adaptive Gain Scaling Control
12:00 - 14:00 h.	Lunch	
14:00 - 15:00 h.	**Invited talk 3: *Dance Partner Robots and a Co-worker Robot PaDY*** **Kazuhiro Kosuge** **Session Chair: Maciej Ogorzalek**	
	Session 11: Hardware Security (Chair: Odysseas K)	Session 12: Machine learning for SoC Design (Chair: Luc Claesen)
15:00 - 15:20 h.	A Hardware-based Framework for Secure Firmware Updates on Embedded Systems	A Machine Learning-Based Framework for Throughput Estimation of Time-Varying Applications in Multi-Core Servers
15:20 - 15:40 h.	Attacking Real-time MPSoCs:Preemptive NoCs are Vulnerable	CongestionNet : Routing Congestion Prediction Using Deep Graph Neural Networks
16:00 - 17:00 h.	Closing Session	

06 OCTOBER

VLSI SoC 2019 Program (Schedule of activities) **(Hall UNSAC Museum)**

15:00 - 16:00	Steering Committee Meeting
16:00 - 18:00	Technical Program Committee Meeting
18:00 - 19:30	IFIP Working Group 10.5 Meeting

07 OCTOBER

08:40 - 09:00	Opening ceremony
09:00 - 10:00	**Keynote 1: "Open, Secure, Near-Sensor Analytics: A Parallel Ultra-Low Power (PULP) Approach"** Professor Luca Benini, Universita di Bologna (Hall Machu Picchu) Chair: Giovanni De Micheli
10:00 - 10:30	Coffee Break
SESSION 1:	**Innovations in IC Design in FDSOI CMOS (Hall Machu Picchu)** Chair: Andrei Vladimirescu
10:30 - 10:50	New design of analog and mixed-signal cells using back-gate cross-coupled structure Gilles Jacquemod and Zhaopeng Wei
10:50 - 11:00	A Distributed Body-Biasing Strategy for Asynchronous Circuits Laurent Fesquet, Yoan Decoudu, Alexis R. Iga, Thiago Ferreira de Paiva Leite, Otto Rolloff, Mamadou Diallo, Rodrigo Possamai Bastos, Katell Morin-Allory and Sylvain Engels
11:00 - 11:30	Benefits of an FD-SOI Feature: Optimal Power Budget of Wireless Links through Phase Noise Tuning Yann Deval, Andreia Cathelin, R. Guillaume, A. Ait Ihda, H. Lapuyade and Francois Rivet
11:30 - 11:50	Does FDSOI bring added value for new connectivity challenges? Didier Belot

12:00 - 14:00	Lunch
14:00 - 15:00	**Invited Talk 1: "Designing Application Specific Machine Learning/Deep Learning Cores"** Prof. Claudionor Coelho Google/ML/DL Sr Research Scientist (Hall Machu Picchu) Chair: Carlos Silva-Cárdenas
SESSION 3:	**Computer-Aided Design (Hall Machu Picchu)** Chair: Srinivas Katkoori
15:00 - 15:20	Automated Synthesis of Multi-Port Memories and Control Hunter Nichols, Michael Grimes, Jennifer Sowash, Jesse Cirimelli-Low and Matthew Guthaus
15:20 - 15:40	Approximate Arithmetic Circuit Design Using a Fast and Scalable Method Qi Lu, Amir Masoud Gharehbaghi and Masahiro Fujita
15:40 - 16:00	An ILP-based Optimization Method for Radiation Hardened Register and ECC Mixed Architectures Keisuke Inoue
16:00 - 16:50	Poster Session + Coffee Break
16:50 - 18:10	Young Professional + SIGDA Diversity Session
19:30	Welcome cocktail

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10:00 - 10:30	Coffee Break
SESSION 2:	**Circuits and Systems for Signal Processing and Communications (Hall Tipon)** Chair: H. Fatih Ugurdag
10:30 - 10:50	An Associativity-Agnostic in-Cache Computing Architecture Optimized for Multiplication Marco Rios, William Simon, Alexandre Levisse, Marina Zapater and David Atienza
10:50 - 11:00	Hardware Considerations for Selection Networks Kenneth Peter, Lars Svensson, Christoffer Fougstedt and Per Larsson-Edefors
11:00 - 11:30	A Mixed-Signal Offset-Compensation System for Multi-Gbit/s Optical Receiver Frontends Laszlo Szilagyi, Jan Pliva, Ronny Henker and Frank Ellinger
11:30 - 11:50	Lossless Look-Up Table Compression for Hardware Implementation of Transcendental Functions Y. Serhan Gener, Sezer Goren and H. Fatih Ugurdag

12:00 - 14:00	Lunch
14:00 - 15:00	**Invited Talk 1: "Designing Application Specific Machine Learning/Deep Learning Cores"** Prof. Claudionor Coelho Google/ML/DL Sr Research Scientist (Hall Machu Picchu) Chair: Carlos Silva-Cárdenas
SESSION 4:	**Variability, Reliability and Test - 1 (Hall Tipon)** Chair: Matteo Sonza Reorda
15:00 - 15:20	Software-Based Self-Test for Transition Faults: a Case Study Matteo Sonza Reorda, Michelangelo Grosso, Salvatore Rinaudo and Andrea Casalino
15:20 - 15:40	Implementation-Independent Functional Test Generation for RISC Microprocessors Adeboye Stephen Oyeniran, Raimund Ubar, Maksim Jenihhin and Jaan Raik
15:40 - 16:00	Minimum Energy FinFET Schmitt Trigger Design Considering Process Variability Leonardo Moraes, Cristina Meinhardt, Alexandra Lackmann Zimpeck and Ricardo Reis
16:00 - 16:50	Poster Session + Coffee Break
16:50 - 18:10	Young Professional + SIGDA Diversity Session
19:30	Welcome cocktail

08 OCTOBER

09:00 - 10:00	**Keynote 2: "Solving Scalability Problems in EDA by Using Optimization and Machine Learning"** Professor Laleh Behjat, Schulich School of Engineering (Hall Machu Picchu) Chair: Pierre Emmanuel Gaillardon
10:00 - 10:30	Coffee Break
SESSION 5:	**Silicon-Proven Multiprocessor SoC Design Strategies (Hall Machu Picchu)** Chair: Gerhard Fettweis
10:30 - 10:50	Challenges and Solutions for Future-Proof Embedded Vision and AI Processors Yankin Tanurhan, Tom Michiels, Eino Jacobs, Joep Boonstra, Chuck Pilkington and Pierre Pauli
10:50 - 11:00	A 0.80 pJ/flop, 1.24 Tflop/sW 8-to-64 bit Transprecision Floating-Point Unit for a 64 bit RISC-V Processor in 22 nm FD-SOI Stefan Mach, Fabian Schuiki, Florian Zaruba and Luca Benini
11:00 - 11:30	KAVUAKA: A Low Power Application Specific Hearing Aid Processor Lukas Gerlach, Guillermo Paya-Vaya and Holger Blume
11:30 - 11:50	5G-and-Beyond Scalable Machines Francisco Veirano, Pablo Pérez, Sebastián Besio, Pablo Castro, Fernando Silveira,
12:00 - 14:00	Lunch

14:00 - 15:00	**Invited Talk 2: "5G Radio Frequency Front-End: be wide-band, be low-power, be low-cost! "** Professor Francois Rivet, University of Bordeaux, France (Hall Machu Picchu) Chair: Ricardo Reis
SESSION 7:	**Embedded Systems Design (Hall Machu Picchu)** Chair: Michael Huebner
15:00 - 15:20	SURF: Self-aware Unified Runtime Framework for Parallel Programs on Heterogeneous Mobile Architectures Chenying Hsieh, Ardalan Amiri Sani and Nikil Dutt
15:20 - 15:40	Arbitrary-Precision Convolutional Neural Networks on Low-Power IoT Processors Valentino Peluso, Matteo Grimaldi and Andrea Calimera
15:40 - 16:00	PhD Forum Introduction (Hall Machu Picchu)
16:00 - 16:50	PhD Forum + Student forum + Coffee Break
16:50 - 18:20	Industry Panel: "Digital transformation: key enabling technologies and their industrial perspectives"
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09:00 - 10:00	**Keynote 2: "Solving Scalability Problems in EDA by Using Optimization and Machine Learning"** Professor Laleh Behjat, Schulich School of Engineering (Hall Machu Picchu) Chair: Pierre Emmanuel Gaillardon
10:00 - 10:30	Coffee Break
SESSION 6:	**Prototyping (Hall Tipon)** Chair: Graziano Pravadelli
10:30 - 10:50	Engineering of an Effective Automatic Dynamic Assertion Mining Platform Tara Ghasempouri, Jan Malburg, Alessandro Danese, Graziano Pravadelli, Goerschwin Fey and Jaan Raik
10:50 - 11:00	SEARS: A Statistical Error and Redundancy Analysis Simulator Atishay, Ankit Gupta, Rashmi Sonawat, Helik Kanti Thacker and Prasanth B
11:00 - 11:30	Non-intrusive Fault Injection Techniques for Efficient Soft Error Vulnerability Analysis Vitor Bandeira, Felipe Rosa, Ricardo Reis and Luciano Ost
11:30 - 11:50	Domain-Specific Architecture for IMU Array Data Fusion Owais Waheed and Ibrahim Elfadel
12:00 - 14:00	Lunch
14:00 - 15:00	**Invited Talk 2: "5G Radio Frequency Front-End: be wide-band, be low-power, be low-cost! "**

Professor Francois Rivet, University of Bordeaux, France (Hall Machu Picchu)
Chair: Ricardo Reis

SESSION 8: **Low-power and Analog IC Design (Hall Tipon)**
Chair: Alberto Macii

15:00 - 15:20 The Impact of Turbo Frequency on the Energy, Performance, and Aging of Parallel Applications
Arthur Lorenzon, Sandro Matheus Marques, Thiarles Soares Medeiros, Fábio Rossi, Marcelo Caggiani Luizelli, Antonio Carlos Schneider Beck Filho and Alessandro Girardi

15:20 - 15:40 Performance Analysis of a Comparator Based Mixed-Signal Control Loop in 28 nm CMOS
Florian Protze, Martin Kreißig and Frank Ellinger

15:40 - 16:00 PhD Forum Introduction (Hall Machu Picchu)

16:00 - 16:50 PhD Forum + Student forum + Coffee Break

16:50 - 18:20 Industry Panel: "Digital transformation: key enabling technologies and their industrial perspectives"

19:30 - 22:00 Gala Dinner

09 OCTOBER

09:30 - 10:30	**Keynote Speech: "Electronic Design Automation and Machine Learning Hardware"** Raul Camposano, CEO of Sage (Hall Machu Picchu) Chair: Victor Grimblatt
10:30 - 11:00	Coffee Break
SESSION 9:	**Emerging Technologies (Hall Machu Picchu)** Chair: Ian O' Connor
11:00 - 11:20	A Product Engine for Energy-Efficient Execution of Binary Neural Networks Using Resistive Memories Joao Vieira, Edouard Giacomin, Yasir Mahmood Qureshi, Marina Zapater, Xifan Tang, Shahar Kvatinsky, David Atienza and Pierre-Emmanuel Gaillardon
11:20 - 11:40	Memory Sizing of a Scalable SRAM In-Memory Computing Tile Based Architecture Roman Gauchi, Maha Kooli, Pascal Vivet, Jean-Philippe Noel, Edith Beigné, Subhasish Mitra and Henri-Pierre Charles
11:40 - 12:00	A Predictive Process Design Kit for Three-Independent-Gate Field-Effect Transistors Ganesh Gore, Patsy Cadareanu, Edouard Giacomin and Pierre-Emmanuel Gaillardon
12:00 - 14:00	Lunch

14:00 - 15:00	**Invited Talk 3: "Dance Partner Robots and a Co-worker Robot PaDY"** Professor Kazuhiro Kosuge Tohoku University, Japan (Hall Machu Picchu) Chair: Maciej Ogorzalek
SESSION 11:	**Hardware Security (Hall Machu Picchu)** Chair: Odysseas K
15:00 - 15:20	A Hardware-based Framework for Secure Firmware Updates on Embedded Systems Solon Falas, Charalambos Konstantinou and Maria K. Michael
15:20 - 15:40	Attacking Real-time MPSoCs:Preemptive NoCs are Vulnerable Bruno Endres Forlin, Cezar Rodolfo Wedig Reinbrecht and Johanna Sepulveda
16:00	Clossing session (Hall Machu Picchu)

09 OCTOBER

09:30 - 10:30	**Keynote Speech: "Electronic Design Automation and Machine Learning Hardware"** Raul Camposano, CEO of Sage (Hall Machu Picchu) Chair: Victor Grimblatt
10:30 - 11:00	Coffee Break
SESSION 10:	**Variability, Reliability and Test - 2 (Hall Tipon)** Chair: Salvador Mir
11:00 - 11:20	Evaluation of SET under Process Variability on FinFET Multi-level Design Leonardo H. Brendler, Alexandra L. Zimpeck, Cristina Meinhardt and Ricardo Reis
11:20 - 11:40	A Simplified Layout-Level method for Single Event Transient Faults Susceptibility on Logic Gates Rafael Schvittz, Denis Franco, Paulo F. Butzen and Leomar Rosa Jr
11:40 - 12:00	An NBTI-Aware Digital Low-Dropout Regulator with Adaptive Gain Scaling Control Soner Seckiner, Longfei Wang and Selcuk Kose
12:00 - 14:00	Lunch
14:00 - 15:00	**Invited Talk 3: "Dance Partner Robots and a Co-worker Robot PaDY"** Professor Kazuhiro Kosuge Tohoku University, Japan (Hall Machu Picchu) Chair: Maciej Ogorzalek

SESSION 12: **Machine learning for SoC Design (Hall Tipon)**
Chair: Luc Claesen

15:00 - 15:20 A Machine Learning-Based Framework for Throughput Estimation of Time-Varying Applications in Multi-Core Servers
Arman Iranfar, Wellington Silva De Souza, Marina Zapater, Katzalin Olcoz, Samuel Xavier-de-Souza and David Atienza

15:20 - 15:40 CongestionNet : Routing Congestion Prediction Using Deep Graph Neural Networks
Robert Kirby, Saad Godil, Rajarshi Roy and Bryan Catanzaro

16:00 Closing session (Hall Machu Picchu)

Posters VLSI SOC 2019

#	Authors	Title
1	Atif Yasin, Tiankai Su, Sebastien Pillement and Maciej Ciesielski	Functional Verification of Hardware Dividers using Algebraic Model
2	Renato Feitoza, Manuel Barragan and Salvador Mir	Reduced-Code Techniques for On-Chip Static Linearity Test of SAR ADCs
3	Chenhao Gu, Leilei Huang, Xiaoyang Zeng and Yibo Fan	A Micro-Code-Based Hardware Architecture of Integer Motion Estimation for HEVC
4	Stavros Limnaios, Nicolas Sklavos and Odysseas Koufopavlou	Lightweight Efficient Simeck32/64 Crypto-Core Designs and Implementations, for IoT Security
5	Adil Brik, Lioua Labrak, Laurent Carrel, Ian O'Connor and Ramy Iskander	Fast extraction of predictive models for integrated circuits using n-performance Pareto fronts
6	Rafael Billig Tonetto, Douglas Maciel Cardoso, Marcelo Brandalero, Luciano Agostini, Gabriel Nazar, José Rodrigo Azambuja and Antonio Carlos Schneider Beck	A Knapsack Methodology for Hardware-based DMR Protection against Soft Errors in Superscalar Out-of-Order Processors
7	Ashfakh Ali, Sai Kiran Lade, Arpan Jain and Zia Abbas	A 47nW, 0.7-3.6V wide Supply Range, Resistor Based Temperature Sensor for IoT Applications
8	Denis Nunes, Silvio Fernandes and Marcio Kreutz	Optimizing an Architecture with Software Pipelining Strategies
9	Bin Wu and Matthew Guthaus	Bottom-Up Approach for High Speed SRAM Word-line Buffer Insertion Optimization
10	Alberto Bosio, W Javier Perez H and Ernesto Sanchez	Exploiting Approximate Computing to Increase System Lifetime
11	Shahzad Muzaffar and Ibrahim Elfadel	Double Data Rate Dynamic Edge-Coded Signaling for Low-Power IoT Communication
12	Andrea Bocco, Tiago T. Jost, Albert Cohen, Florent de Dinechin, Yves Durandand Christian Fabre	Byte-aware Floating-point Operations through a UNUM Computing Unit

13	Kevin Cáceres Albinagorta, Calebe Conceicão, Carlos Silva Cardenas and Ricardo Reis	Exploring area and total wirelength using a cell merging technique
14	Aleksa Damljanovic, Cemil Cem Gursoy, Maksim Jenihin and Giovanni Squillero	On NBTI-induced Aging Analysis in IEEE 1687 Reconfigurable Scan Networks
15	Rafaella Elia, George Plastiras and Theocharis Theocharides	Towards an Embedded and Real-Time Joint Human-Machine Monitoring Framework: Dataset Optimization Techniques for Anomaly Detection

Instructions

Dear Author of a VLSI-SoC Poster,

We would like to remind you that, as your paper will be presented as POSTER in the event, you should prepare the poster considering the following:

1. To fit on a board measuring 950mm (width) x 1100mm (height).
2. Include the VLSI-SoC 2019 logo in the poster.
3. Please be prepared to have your poster set up at noon on Monday, October 7th
4. You should be close to your poster during the whole Poster Session and be prepared to answer possible questions.
5. Poster Session is scheduled to Monday, October 7th, afternoon
6. The VLSI-SoC Program is available in the VLSI-SoC 2019 website https://vlsi-soc.pe

Remember that only the accepted papers presented in the event will be included in the official proceedings to be published at IEEE XPlore. A NO-SHOW will imply that the paper will be EXCLUDED from the official proceedings.

See you in Cusco!!!

The Organizing Committee of VLSI-SoC 2019

Papers PHD Forum VLSI SOC 2019

#	Authors	Title
1	Denis F. L. Nunes and Marcio Kreutz	Using SDN Strategies to Improve Resource Management On a NoC
2	Malek Souilem, Jai Narayan Tripathi, Wael Dghais and Hamdi Belgacem	I/O Buffer Modelling for Power Supplies Noise Induced Jitter under Simultaneous Switching Outputs (SSO)
3	Diego Silva, Orlando Verducci and Duarte de Oliveira	Implementation of DES Algorithm in New Non-Synchronous Architecture Aiming DPA Robustness
4	Wellington Souza, Arman Iranfar, Anderson Bráulio Nóbrega da Silva, Marina Zapater Sancho, Samuel Xavier de Souza, Katzalin Olcoz Herreroand David Atienza Alonso	A QoS and container-based approach for energy saving and performance profiling in multi-core servers
5	Diego V. C. Nascimento, Kyriakos Georgiou, Kerstin Eder and Samuel Xavier-de-Souza	Exploiting guard band limits for energy gains in MPSoCs
6	Demetrios Coutinho, Kyriakos Georgiou, Kerstin Eder, Jose Nunez-Yanez and Samuel Xavier-De-Souza	Performance and Energy Efficiency Trade-Offs in Single-ISA Heterogeneous Multi-Processing for Parallel Applications
7	Rafael Schvittz, Paulo F. Butzen and Leomar Rosa Jr	Exploring Logic Gates Layout to Improve the Accuracy of Circuit Reliability Estimation
8	Calebe Conceicao and Ricardo Reis	Netlist Optimization by Gate Merging
9	Ettore Napoli, Davide De Caro, Darjn Esposito, Nicola Petra and Antonio G.M. Strollo	Design of approximate compressors without carry bits to be used in binary multiplier circuits

10	Robert Wittig, Mattis Hasler, Emil Matus and Gerhard Fettweis	Probabilistic Models for Off-Line Arbiters in Embedded Systems
11	Alexandra Lackmann Zimpeck, Cristina Meinhardt, Laurent Artola, Guillaume Hubert, Fernanda Kastensmidt and Ricardo Reis	Circuit-Level Techniques to Mitigate Process Variability and Soft Errors in FinFET Designs
12	Yu-Cheng Chen, Vincent Mooney and Santiago Grijalva	A Hybrid Attack Model for Cyber-Physical Security Assessment in Electricity Grid
13	Alexis Rodrigo Iga Jadue, Sylvain Engels and Laurent Fesquet	A Digital Event-Based Strategy for ASK demodulation